Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

174. (previously amended)

A method of controlling the conduction of a pair of isolation transistors in a sense amplifier responsive to an array, comprising:

rendering the pair of transistors conductive during a write operation with a control signal that is a boosted version of the voltage used by the array; and

rendering the pair of transistors nonconductive by removing said control signal.

175. (previously amended)

The method of claim 174 wherein said rendering the pair of transistors conductive includes rendering the transistors conductive with a control signal that is approximately a Vth higher than the voltage used by the array.

176. (previously amended)

The method of claim 174 wherein said rendering the transistors conductive includes rendering the transistors conductive with a control signal that enables the full voltage representative of a logic level one to be written to the array.

177. (currently amended)

A method of controlling the conduction of at least one isolation transistor in a sense amplifier responsive to an array, comprising:

rendering the transistor conductive with a control signal that enables a full Vcc to be conducted by the isolation transistor during a write operation, said control signal being a boosted version of the voltage used by the array; and

rendering the transistor nonconductive by removing said control signal.

178. (previously amended)

The method of claim 177 wherein said rendering the transistor conductive includes rendering the transistor conductive with a control signal that is approximately a Vth higher than Vcc.

179. (currently amended)

A method of enabling a write to a memory array of the full voltage representative of a logic level one using a sense amplifier in which the sense amplifiers are located inside the isolation transistors, comprising:

rendering the isolation transistors conductive with a control signal that compensates for the voltage drop across the isolation transistors said control signal being a boosted version of the voltage used by the array.

180. (previously amended)

The method of claim 179 wherein said rendering includes rendering the isolation transistors conductive with a control signal that is approximately a Vth higher than the voltage used to represent a logic level one.

181. (previously added)

The method of claim 180 wherein said control signal is approximately Vth plus Vcc.